User Manual

MSC TDC-MACH 330

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1 Introduction

MSC Vertriebs GmbH has many years of experience in the development of high precision Time to Digital Converters (TDCs). Our first TDC was developed in 1990 and implemented in a cost-effective CMOS Gate Array technology.

This manual describes the TDC-Mach330, an innovative, PLD-based Time to Digital Converter. Designed specially for a programmable logic device of the Lattice MachXO-family the TDC is born in our company's state of the art programming center, tested and delivered to you in a 14x14mm TQFP100, a 20x20mm TQFP144 or an 8x8mm csBGA100 package, each with 0,5mm pitch.

Supplied with 3.3V the TDC-Mach330 achieves a typical resolution of up to 115ps (LSB). This resolution cannot be achieved using conventional FPGA- or PLD-based time measuring components. The integrated measurement principle allows high-precision time difference measurement at very low prices. The TDC-Mach330 is perfectly suited for applications like distance measurement using laser, phase measurement, ultrasonic positioning, temperature measurement, etc. which have been implemented successfully with our Gate Array based TDCs many times before.

Please contact us! We are keen on satisfying your wishes.

2 Features

Channels:	one channel for Start-Stop measurements, consisting of one Start- and one Stop-input. Both inputs trigger on rising edges.
Resolution LSB: (V_{CC} = 3.3V, T_A = 25°C)	115ps
Resolution RMS: (V_{CC} = 3.3V, T_A = 25°C)	250ps *)
Measurement range:	$(1.5*t_{CAL}+100ns) - 2^{15}*t_{CAL}$
Calibration Clock:	external crystal clock required, $3MHz \leq f_{CAL} \leq 4MHz$
Calibration measurement:	automatically after time measurement or stand-alone
Processor interface:	parallel interface: 8 bit data / 3 bit address, serial interface: 4 wire SPI, flags for end of measurement and overflow
Internal memory:	result of time measurement: three 16 bit values, result of calibration measurement: two 16 bit values
Configuration:	programmable via processor interface
Measurement improvement:	Auto Noise Unit
Technology:	Lattice MachXO-PLD
Voltage range:	V_{CC} = 3.0V - 3.6V
Temperature range:	T_A = 0°C - 70°C
Package:	TQFP100 (14 x 14mm), TQFP144 (20 x 20mm) or csBGA100 (8 x 8mm), each with 0.5mm pitch
I/Os:	LVCMOS (3.3V), Outputs = 8mA
Sleep Mode:	Allows up to 1000x static current reduction

*) $f_{CAL} = 1/t_{CAL} = 4MHz$

3 Block Diagram

Figure 3.1 shows the block diagram of the TDC-Mach330.

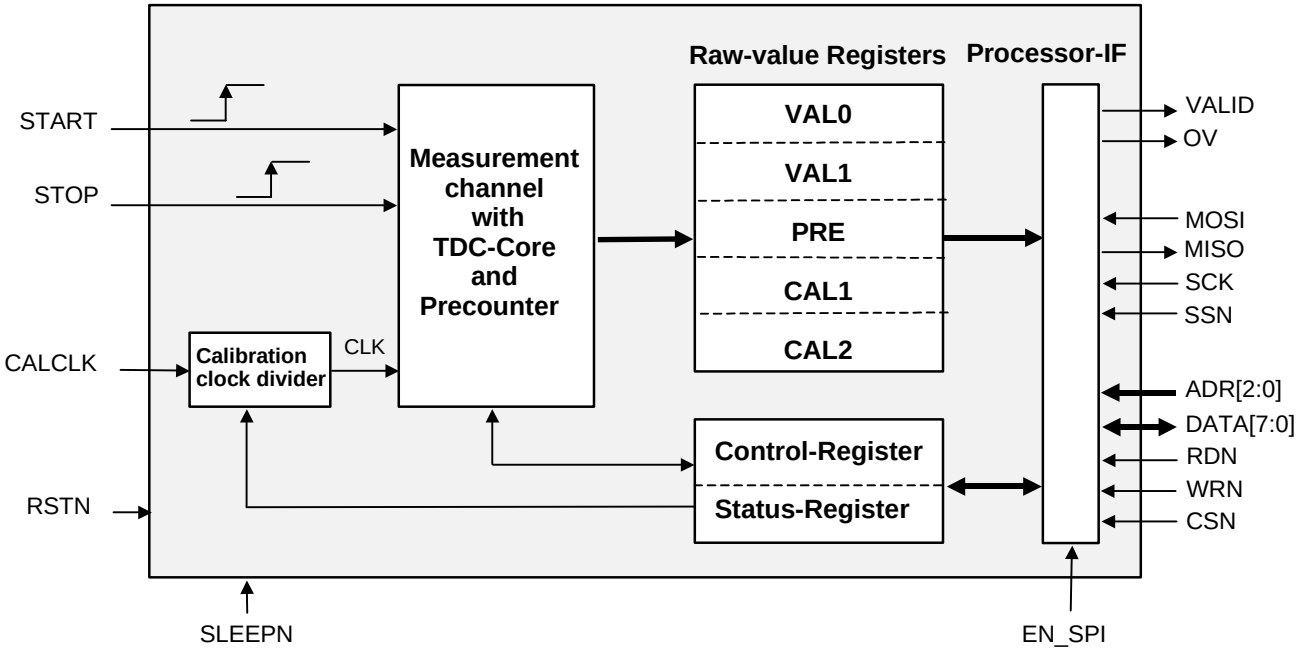


Figure 3.1: TDC-Mach330 Block Diagram

The TDC offers one **Measurement channel** with **TDC-Core** and **Precounter** for time measurements between one start- and one stop-signal. The uncalibrated measurement values are stored in the **Raw-value registers**. Two flags indicate either the end of a measurement or an overflow of the TDC-Core or Precounter. After the end of a measurement the raw-values have to be read out either parallel or serial via the **Processor interface**. The calibration and calculation of the measurement's result has to be done outside the TDC (e.g. by using a microcontroller).

The configuration of the TDC is done by writing the **Control-Register** via the processor interface. Status information can be accessed by reading the **Status-Register**.

The calibration clock, necessary for the calibration of the uncalibrated measurement values, has to be supplied by an externally generated crystal clock. The crystal clock is divided by the internal **calibration clock divider** circuit.

Sleep Mode allows up to 1000x static current reduction.

4 Packages, Pin- and Ball-Configurations

4.1 Thin Quad Flat Package (TQFP)

Figure 4.1 shows the TDC's Thin Quad Flat Package with either 100 pins (TQFP100, 14 x 14mm) or 144 pins (TQFP144, 20 x 20mm). The package dimensions are specified in Table 4.1 and Table 4.2

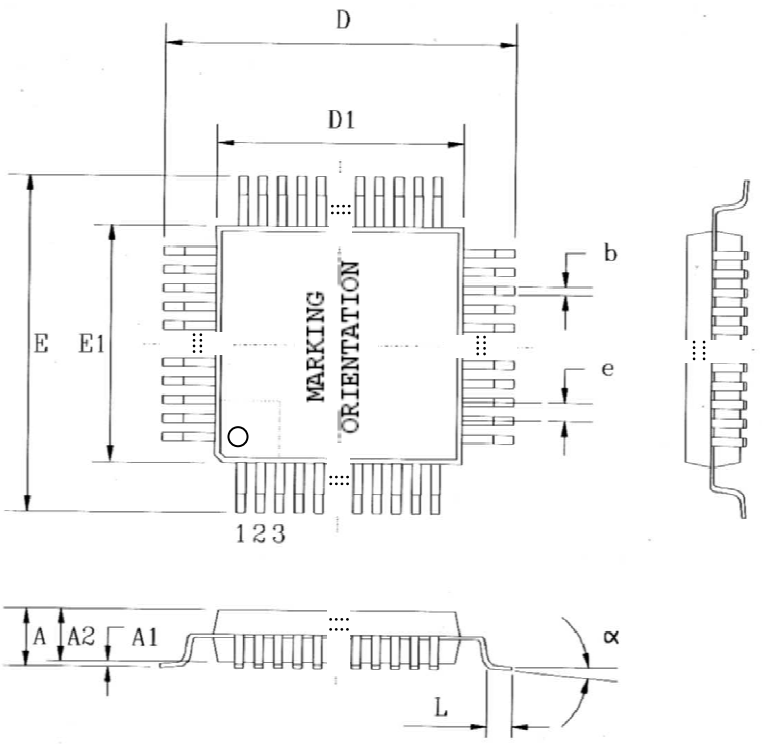


Figure 4.1: Thin Quad Flat Package

	E1 / D1	A	A1	A2	e	b	L	α	D / E
min	-	-	0,05	1,35	-	0,17	0,45	0°	-
typ	14,00	-	-	1,40	0,50	0,22	0,60	-	16,00
max	-	1,60	0,15	1,45	-	0,27	0,75	7°	-

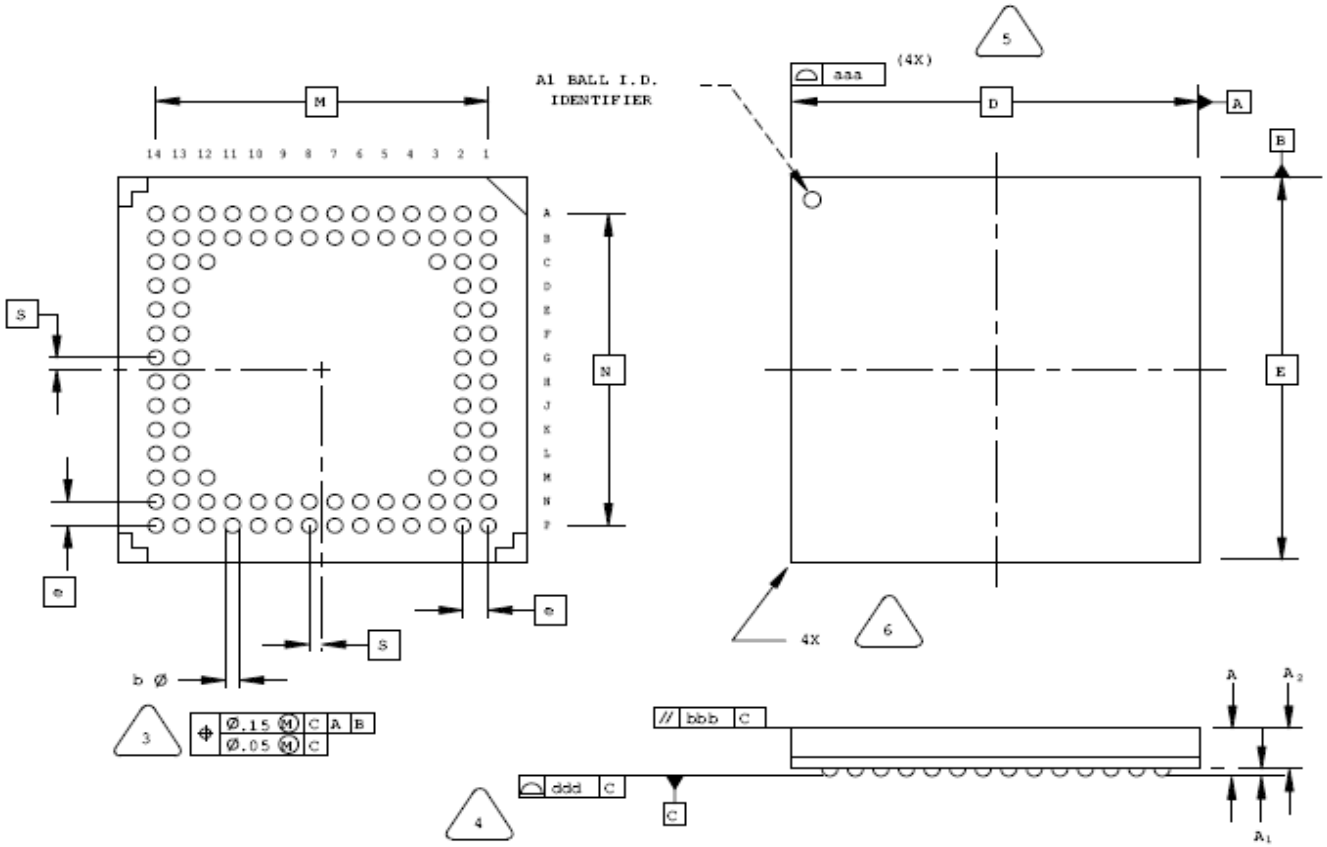
Table 4.1: TQFP100 Package Dimensions [mm]

	E1 / D1	A	A1	A2	e	b	L	α	D / E
min	-	-	0,05	1,35	-	0,17	0,45	0°	-
typ	20,00	-	-	1,40	0,50	0,22	0,60	-	22,00
max	-	1,60	0,15	1,45	-	0,27	0,75	7°	-

Table 4.2: TQFP144 Package Dimensions [mm]

4.2 Chip Scale Ball Grid Array (csBGA)

Figure 4.2 shows the TDC's space saving Chip Scale Ball Grid Array with 100 balls (csBGA100, 8 x 8mm). The package dimensions are also specified in Figure 4.2.



NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3 DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C

4 PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5 BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.

6 EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

SYMBOL	MIN.	NOM.	MAX.
A	0.90	1.23	1.35
A1	0.15	-	-
A2	-	-	1.10
D/E	8.00 BSC		
M/N	6.50 BSC		
S	0.25 BSC		
b	0.25	0.30	0.35
e	0.50 BSC		
aaa	-	-	0.10
bbb	-	-	0.10
ddd	-	-	0.08

Figure 4.2: csBGA100 Package and Dimensions [mm]

4.3 Pin and Ball Configurations

Table 4.3, Table 4.4 and Table 4.5 show the TDC's pin and ball configurations. Pin resp. ball names of low active signals end with 'N'.

Pin No.	Pin Name	I/O	Function
10, 24, 29, 35, 41, 60, 74, 80, 88, 90, 92	V_{CC}	-	Power supply: 3.0V - 3.6V
12, 25, 28, 30, 40, 42, 62, 75, 81, 84, 86, 93	GND	-	Ground
5	VALID	Out, 8mA	0 : No valid data for readout 1 : End of measurement: Raw-value registers contain valid data for readout
11	START	In	Start-input, triggers on rising edges
13	STOP	In	Stop-input, triggers on rising edges
32	RSTN	In, internal pull-up	Power-on reset (low active)
36	SSN	In	SPI: Slave select. When SSN = 1, then SPI in reset
38	CALCLK	In	Input for crystal clock: 3MHz $\leq f_{CALCLK} \leq$ 32MHz
48	SLEEPN	In, internal pull-up	0 : Sleep mode 1 : Normal mode
58	DATA0	Bidi, 8mA	Bit0 data bus
61	DATA1	Bidi, 8mA	Bit1 data bus
63	DATA2	Bidi, 8mA	Bit2 data bus
64	MOSI	In	SPI: Master out slave in
65	DATA3	Bidi, 8mA	Bit3 data bus
66	EN_SPI	In	0 : parallel interface 1 : SPI
67	DATA4	Bidi, 8mA	Bit4 data bus
68	MISO	Tristate Out, 8mA	SPI: Master in slave out. When pin SSN = 1: tristate
69	DATA5	Bidi, 8mA	Bit5 data bus
71	DATA6	Bidi, 8mA	Bit6 data bus
73	DATA7	Bidi, 8mA	Bit7 data bus
77	ADR0	In	Bit0 address bus
79	ADR1	In	Bit1 address bus
82	ADR2	In	Bit2 address bus
85	SCK	In	SPI-clock: $f_{SCK} \leq$ 25MHz
89	RDN	In, internal pull-up	Read strobe (low active)
95	WRN	In, internal pull-up	Write strobe (low active)
97	CSN	In, internal pull-up	Chip select (low active)
99	OV	Out, 8mA	0 : TDC-Core and Precounter ok 1 : Overflow of TDC-Core or Precounter
1, 2, 3, 4, 6, 7, 8, 9, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 26, 27, 31, 33, 34, 37, 39, 43, 44, 45, 46, 47, 49, 50, 51, 52, 53, 54, 55, 56, 57, 59, 70, 72, 76, 78, 83, 87, 91, 94, 96, 98, 100	NC	-	Do not connect!

Notes:
- *All Inputs/Outputs are LVCMOS 3.3V.*
- *When operating via the parallel interface, SCK and MOSI have to be tied to GND and SSN has to be tied to V_{CC}.*
- *When operating via the SPI, DATA[7:0] and ADR[2:0] have to be tied to GND.*

Table 4.3: Pin Function List TQFP100

Pin No.	Pin Name	I/O	Function
10, 21, 26, 38, 52, 53, 63, 82, 93, 98, 117, 128, 129, 135	V_{CC}	-	Power supply: 3.0V - 3.6V
11, 16, 27, 37, 42, 59, 64, 83, 88, 99, 118, 123, 127, 136	GND	-	Ground
4	VALID	Out, 8mA	0 : No valid data for readout 1 : End of measurement: Raw-value registers contain valid data for readout
9	START	In	Start-input, triggers on rising edges
12	STOP	In	Stop-input, triggers on rising edges
49	RSTN	In, internal pull-up	Power-on reset (low active)
55	SSN	In	SPI: Slave select. When SSN = 1, then SPI in reset
58	CALCLK	In	Input for crystal clock: 3MHz $\leq f_{CALCLK} \leq$ 32MHz
70	SLEEPN	In, internal pull-up	0 : Sleep mode 1 : Normal mode
78	DATA3	Bidi, 8mA	Bit3 data bus
80	DATA0	Bidi, 8mA	Bit0 data bus
81	DATA1	Bidi, 8mA	Bit1 data bus
89	DATA2	Bidi, 8mA	Bit2 data bus
92	MOSI	In	SPI: Master out slave in
94	EN_SPI	In	0 : parallel interface 1 : SPI
95	DATA4	Bidi, 8mA	Bit4 data bus
96	MISO	Tristate Out, 8mA	SPI: Master in slave out. When pin SSN = 1, then MISO = tristate
97	DATA5	Bidi, 8mA	Bit5 data bus
103	DATA6	Bidi, 8mA	Bit6 data bus
106	DATA7	Bidi, 8mA	Bit7 data bus
111	ADR0	In	Bit0 address bus
114	ADR1	In	Bit1 address bus
120	ADR2	In	Bit2 address bus
124	SCK	In	SPI-clock: $f_{SCK} \leq$ 25MHz
133	RDN	In, internal pull-up	Read strobe (low active)
139	WRN	In, internal pull-up	Write strobe (low active)
141	CSN	In, internal pull-up	Chip select (low active)
143	OV	Out, 8mA	0 : TDC-Core and Precounter ok 1 : Overflow of TDC-Core or Precounter
1, 2, 3, 5, 6, 7, 8, 13, 14, 15, 17, 18, 19, 20, 22, 23, 24, 25, 28, 29, 30, 31, 32, 33, 34, 35, 36, 39, 40, 41, 43, 44, 45, 46, 47, 48, 50, 51, 54, 56, 57, 60, 61, 62, 65, 66, 67, 68, 69, 71, 72, 73, 74, 75, 76, 77, 79, 84, 85, 86, 87, 90, 91, 100, 101, 102, 104, 105, 107, 108, 109, 110, 112, 113, 115, 116, 119, 121, 122, 125, 126, 130, 131, 132, 134, 137, 138, 140, 142, 144	NC	-	Do not connect!

Notes:
- *All Inputs/Outputs are LVCMOS 3.3V.*
- *When operating via the parallel interface, SCK and MOSI have to be tied to GND and SSN has to be tied to V_{CC}.*
- *When operating via the SPI, DATA[7:0] and ADR[2:0] have to be tied to GND.*

Table 4.4: Pin Function List TQFP144

Ball No.	Pin Name	I/O	Function
P4, P7, B12, B7, B6, B5, A14, H14, P10, G1, P1	V_{CC}	-	Power supply: 3.0V - 3.6V
H1, N2, N4, N3, N10, G14, B13, A10, B8, A4, N9, B9	GND	-	Ground
C2	VALID	Out, 8mA	0 : No valid data for readout 1 : End of measurement: Raw-value registers contain valid data for readout
G2	START	In	Start-input, triggers on rising edges
H2	STOP	In	Stop-input, triggers on rising edges
N5	RSTN	In, internal pull-up	Power-on reset (low active)
N7	SSN	In	SPI: Slave select. When SSN = 1, then SPI in reset
N8	CALCLK	In	Input for crystal clock: 3MHz $\leq f_{CALCLK} \leq$ 32MHz
M12	SLEEPN	In, internal pull-up	0 : Sleep mode 1 : Normal mode
J14	DATA0	Bidi, 8mA	Bit0 data bus
H13	DATA1	Bidi, 8mA	Bit1 data bus
G13	DATA2	Bidi, 8mA	Bit2 data bus
F14	MOSI	In	SPI: Master out slave in
F13	DATA3	Bidi, 8mA	Bit3 data bus
E14	EN_SPI	In	0 : parallel interface 1 : SPI
E13	DATA4	Bidi, 8mA	Bit4 data bus
D14	MISO	Tristate Out, 8mA	SPI: Master in slave out. When SSN = 1: tristate
D13	DATA5	Bidi, 8mA	Bit5 data bus
C13	DATA6	Bidi, 8mA	Bit6 data bus
C12	DATA7	Bidi, 8mA	Bit7 data bus
A12	ADR0	In	Bit0 address bus
A11	ADR1	In	Bit1 address bus
B10	ADR2	In	Bit2 address bus
A8	SCK	In	SPI-clock: $f_{SCK} \leq$ 25MHz
A6	RDN	In, internal pull-up	Read strobe (low active)
A3	WRN	In, internal pull-up	Write strobe (low active)
A2	CSN	In, internal pull-up	Chip select (low active)
A1	OV	Out, 8mA	0 : TDC-Core and Precounter ok 1 : Overflow of TDC-Core or Precounter
B1, C1, D2, D1, E1, E2, F1, F2, J1, J2, K1, K2, L1, L2, M1, M2, N1, M3, P2, P3, P5, P6, N6, P8, P9, P11, N11, P12, N12, P13, P14, N13, N14, M14, L13, L14, M13, K14, K13, J13, C14, B14, A13, B11, A9, A7, A5, B4, B3, C3, B2	NC	-	Do not connect!

Notes:
- *All Inputs/Outputs are LVCMOS 3.3V.*
- *When operating via the parallel interface, SCK and MOSI have to be tied to GND and SSN has to be tied to V_{CC}.*
- *When operating via the SPI, DATA[7:0] and ADR[2:0] have to be tied to GND.*

Table 4.5: Ball Function List csBGA100

5 Measuring Procedure

The TDC-Mach330 provides a measurement channel with TDC-Core with a typical resolution of 115ps (LSB). In addition the TDC has a Precounter for counting the calibration clocks between start and stop of a time measurement.

5.1 Time Measurement

As shown in Figure 3.1 and Figure 5.1, one start- and one stop-input are available for measuring the time differences $\mathbf{t_{RES}}$. Both inputs trigger on rising edges. Each measurement is divided into three stages:

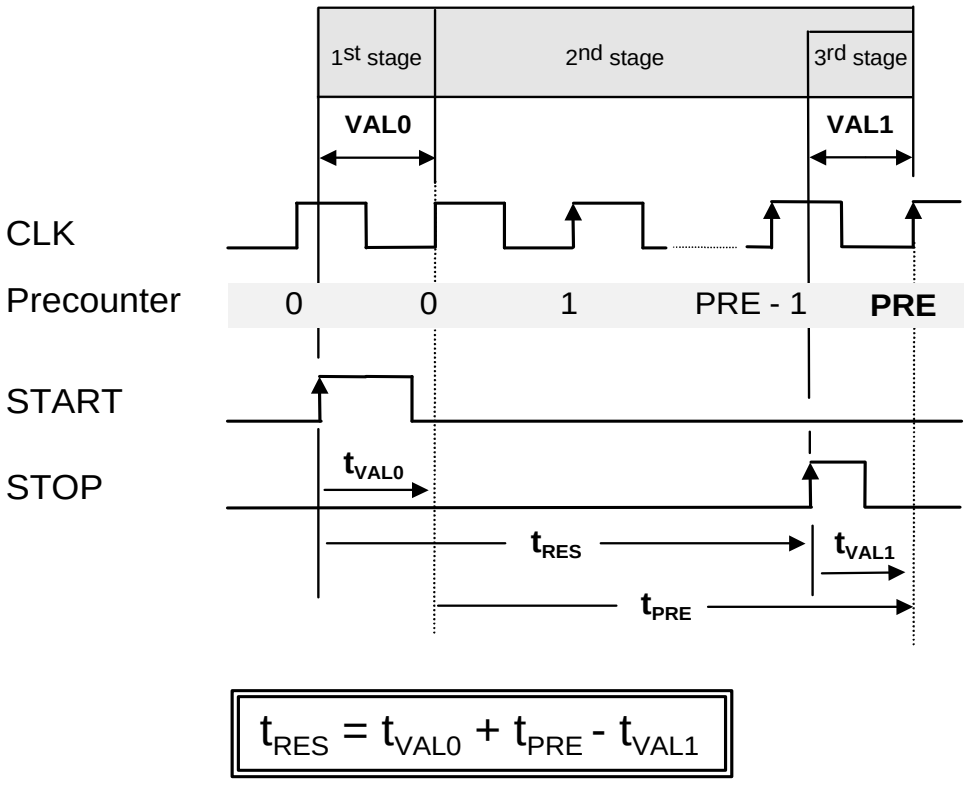


Figure 5.1: Time Measurement

In the first stage of the measurement the TDC-Core measures the time difference $\mathbf{t_{VAL0}}$ between the start-signal and the following rising edge of the divided calibration clock CLK. The result is stored as measurement value **VAL0** in a raw-value register. In the second stage the Precounter counts the clock periods of CLK between the start- and the stop-signal to get the time difference $\mathbf{t_{PRE}}$. The result **PRE** is also stored in a raw-value register. Finally, in the third stage of the measurement, the time difference $\mathbf{t_{VAL1}}$ between the stop-signal and the following rising edge of CLK is measured using the TDC-Core once again. The result is stored as measurement value **VAL1** in a raw-value register.

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The measurement values VAL0 and VAL1 are dependant on the temperature and the supply voltage. Therefore they have to be weighted according to the TDC characteristic (see Figure 5.2). Offset and gradient of the characteristic have to be determined by a so-called **calibration measurement**.

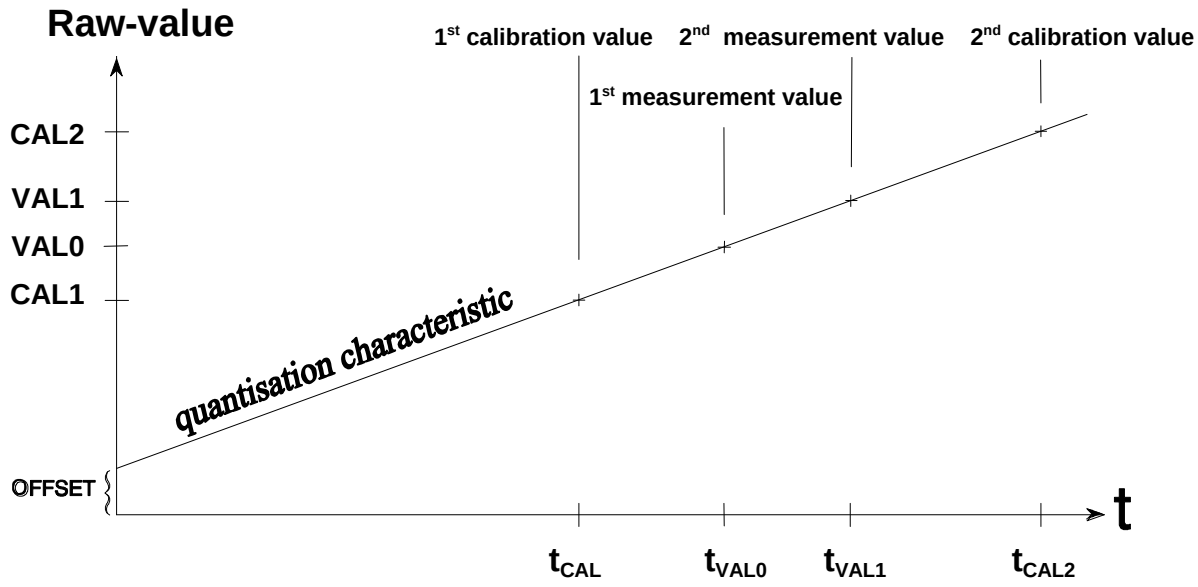


Figure 5.2: Characteristic of the TDC-Core

5.2 Generating Calibration Values

To generate the calibration values **CAL1** and **CAL2**, shown in Figure 5.3, a clock-signal has to be provided at the TDC's pin CALCLK. This clock is the absolute time reference and therefore it must have the precision of a crystal. This crystal clock is divided by the internal calibration clock divider. The resulting calibration clock CLK is measured during a calibration measurement using the TDC-Core.

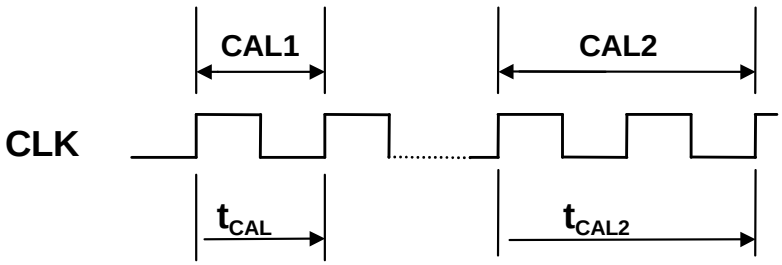


Figure 5.3: Calibration Measurement

During the calibration measurement the length of one and two periods of the divided calibration clock CLK are measured and the resulting calibration values CAL1 and CAL2 are stored just like the measurement value VAL in the raw-value registers. The time periods $\mathbf{t_{CAL}}$ and $\mathbf{t_{CAL2} = 2 * t_{CAL}}$ are well known.

A calibration measurement is performed either automatically after a time measurement or has to be started stand-alone from time to time depending on the required accuracy.

5.3 Result Calculation

The time differences $\mathbf{t_{VAL0}}$, $\mathbf{t_{VAL1}}$ and $\mathbf{t_{PRE}}$ of each measurement stage and the resulting time difference $\mathbf{t_{RES}}$ are calculated using the divided calibration clock period $\mathbf{t_{CAL}}$ and the raw-values **VAL0, VAL1, PRE, CAL1** and **CAL2** in accordance with the TDC's quantisation characteristic shown in Figure 5.2 as follows:

$$\mathbf{(1)} \quad t_{VAL0} = \frac{VAL0 - OFFSET}{CAL2 - CAL1} * t_{CAL}$$

$$\mathbf{(2)} \quad t_{VAL1} = \frac{VAL1 - OFFSET}{CAL2 - CAL1} * t_{CAL}$$

$$\mathbf{(3)} \quad OFFSET = 2 * CAL1 - CAL2$$

$$\mathbf{(4)} \quad t_{PRE} = PRE * t_{CAL}$$

$$\mathbf{(5)} \quad t_{RES} = \left[\frac{VAL0 - VAL1}{CAL2 - CAL1} + PRE \right] * t_{CAL}$$

5.4 General Measurement Cycle

Figure 5.4 shows the flowchart of a general measurement cycle. At the very beginning of a measurement cycle the Calibration Clock Divider's division factor has to be specified within the TDC's Control Register.

The actual measurement cycle is initiated by setting one of three action-bits to '1' within the Control-Register. Either a time measurement with or without a following automatic calibration measurement will be activated or a stand-alone calibration measurement will start.

Activating a time measurement the TDC is ready now for measurement and waits for a start-signal on the start-input START. After start the time measurement stops when the stop-signal hits the stop-input STOP. Now an automatic calibration measurement follows or not. A stand-alone calibration measurement will start immediately after setting the action-bit to '1'.

If the time measurement and/or calibration measurement are completed error-free, the VALID-flag is set to '1' within the Status-Register and at the TDC-pin VALID as well: All the raw-values of the cycle's measurements are ready for readout.

If a time or calibration measurement is not completed error-free because of an overflow of the TDC-Core or the Precounter, then the OV_CORE- or OV_PRE-flag is set to '1' within the Status-Register. In addition the OV-flag at the TDC-pin OV is set to '1'. In this case the raw-value registers contain no valid data for readout.

A general measurement cycle is finished by clearing the corresponding action-bit to '0'. In so doing, all the flags are cleared to '0' and the raw-values are not valid any more.

A following measurement cycle has to be initiated by setting one of three action-bits to '1' once again.

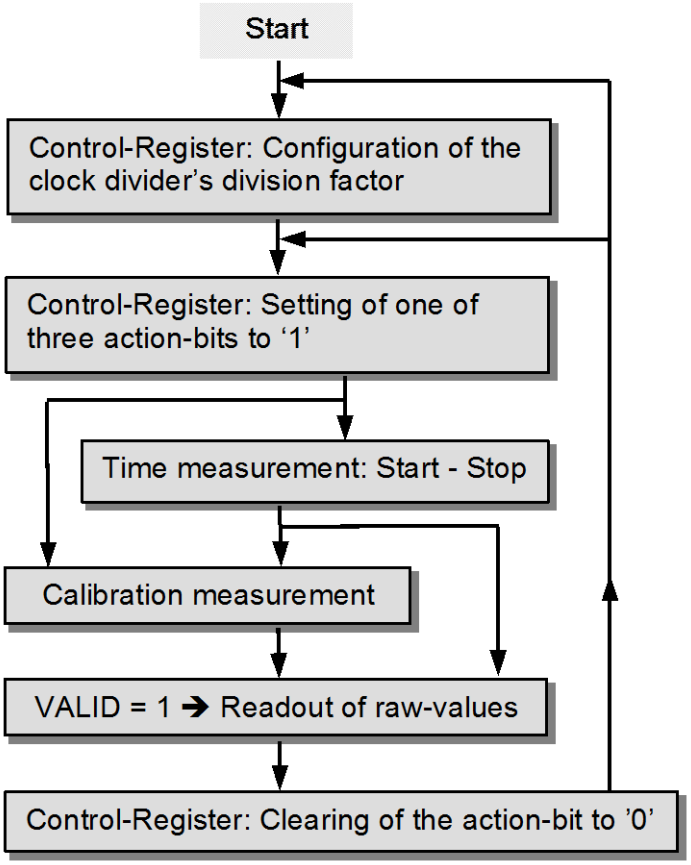

Start
Control-Register: Configuration of the clock divider's division factor
Control-Register: Setting of one of three action-bits to '1'
Time measurement: Start - Stop
Calibration measurement
VALID = 1 ➔ Readout of raw-values
Control-Register: Clearing of the action-bit to '0'

Figure 5.4: General Measurement Cycle Flow

6 Functional Description

6.1 Calibration Clock Divider

Figure 6.1 shows the principle function of the Calibration Clock Divider.

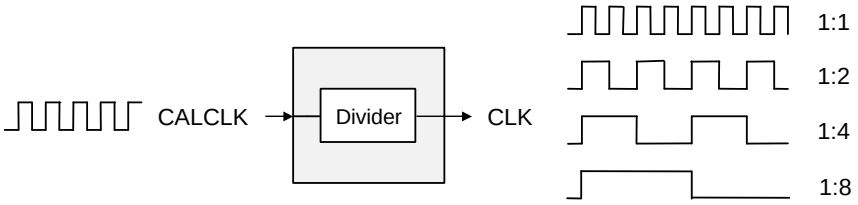


Figure 6.1: Calibration Clock Divider

The external crystal clock CALCLK is divided by the Calibration Clock Divider. The division factor is programmable and can be set to 1, 2, 4 and 8.

CALCLK has to meet the following requirements: $\mathbf{3MHz \leq f_{CALCLK} \leq 32MHz}$

The divided calibration clock CLK is limited to: $\mathbf{3MHz \leq f_{CAL} \leq 4MHz}$

6.2 Measurement Channel

Figure 6.2 shows the block diagram of the measurement channel.

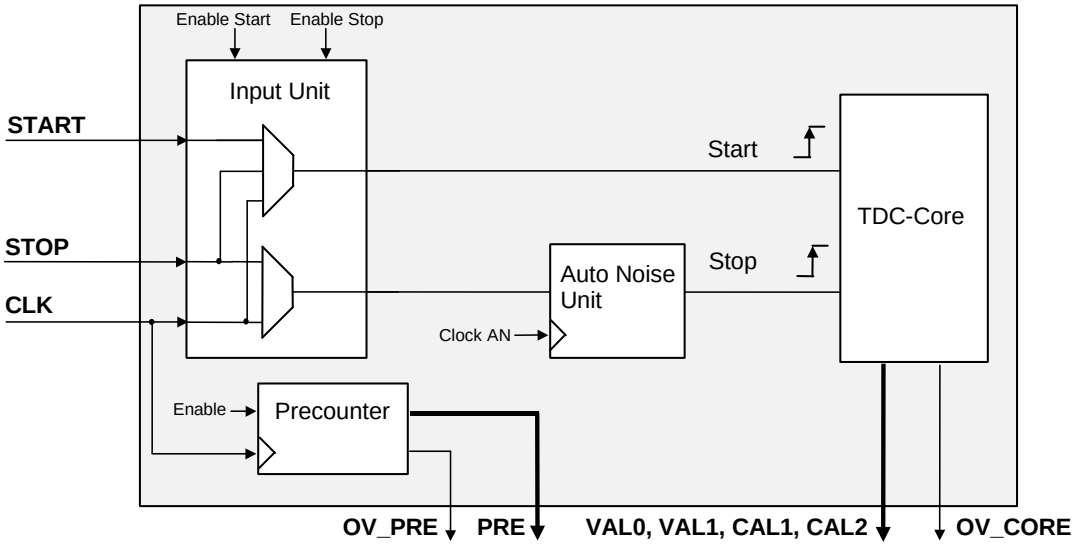


Figure 6.2: Measurement Channel Block Diagram

6.2.1 Input Unit

The Input Unit handles the incoming start-, stop- and calibration clock-signals: The Input Unit decides, which signal (START, STOP or CLK) has to be passed on as a start- or stop-signal to the TDC-Core, depending on the Control-Register's action-bits and on the partial step of the measurement cycle. If there is - for example - no action-bit set to '1' within the Control-Register, then no incoming signal will be passed on to the TDC-Core.

6.2.2 Precounter

The Precounter is enabled by the start-signal and disabled by the stop-signal of a time measurement. It counts the clock periods t_{CAL} of the divided calibration clock CLK between the start-signal and the stop-signal. The width of the resulting precounter value PRE is 15 bit. Therefore the maximum measurement period of the TDC is $t_{max} = 2^{15} * t_{CAL}$ (cp. Appendix 9.4.2).

If the time difference the Precounter has to measure exceeds the maximum measurement period, an overflow OV_PRE will occur: The OV_PRE-flag within the Status-Register and the OV-flag at the TDC-pin OV are set to '1'. Furthermore the ongoing time measurement is aborted including any automatic calibration measurement.

6.2.3 Auto Noise Unit

The characteristic of the TDC is a straight line with offset and upward gradient, which due to the digital measurement procedure possesses quantisation stages - so called LSBs (Least Significant Bits) - with the width of the resolution. For a single measurement one therefore gets a quantisation error of up to one quantisation stage at ideal quantisation. This precision is sufficient for most applications.

A higher precision can be achieved when the measurement of the same time difference is repeated several times and statistical methods are used:

Changing the offset of the characteristic for each single measurement by delaying the stop-signal according to Figure 6.3 causes sampling at different positions of the characteristic. If the same offset is used for the time measurement and the associated calibration measurement, the total offset is eliminated during the result calculation (cp. Chapter 5.3). When averaging all the single measurement results, then all their quantisation errors are averaged as well.

The different delays are generated by the pseudo-random number generator of the Auto Noise Unit. The delays are added to the already existing offset of the channel and can be changed every time you set the action-bit 'clock auto noise' to '1' within the Control-Register. The pseudo-random number generator provides 64 different states each generating another delay. The pseudo-random number generator is cleared on power-on reset only.

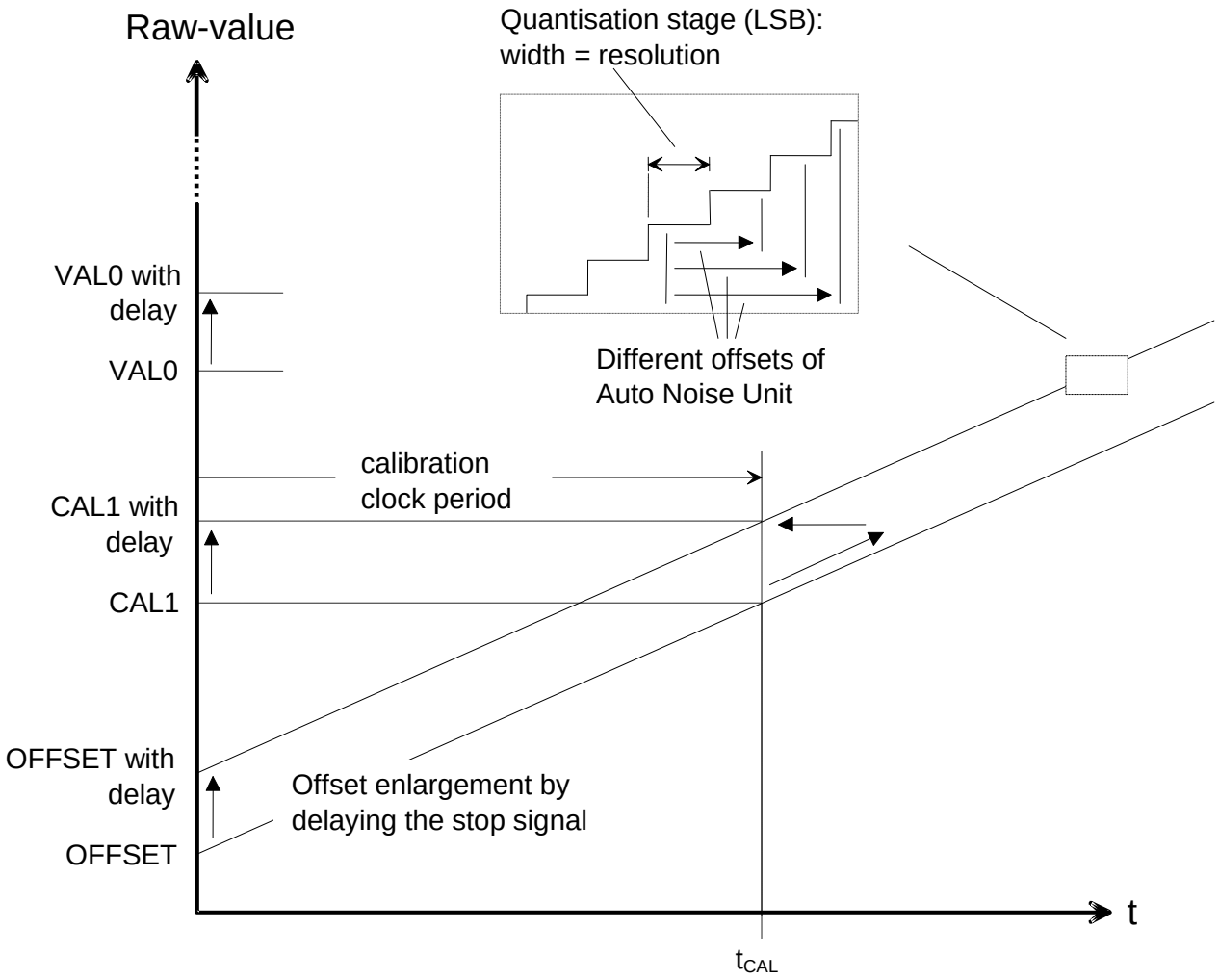


Figure 6.3: Influence of the Auto Noise Unit on the Characteristics of the TDC-Core

6.2.4 TDC-Core

The TDC-core determines the time difference between a start- and a stop-signal with a typical resolution of 115ps (LSB). The TDC-Core stores the resulting measurement- and calibration values in the raw-value registers for readout.

If the time difference exceeds the TDC-Core's typical maximum measurement period of about 4,2µs, an overflow will occur: The OV_CORE-flag within the Status-Register and the OV-flag at the TDC-pin OV are set to '1'. Furthermore the ongoing time- or calibration measurement is aborted immediately.

6.3 Control- and Status-Register

The width of both registers is 8 bit. They are accessible via the processor interface (see Chapter 6.5). For addressing the registers refer to Chapter 7.1.

The Control-Register is read- and writeable. The Status-Register is read-only. For detailed information on the individual register bits refer to Chapter 7.2.

6.4 Raw-Value Registers

The TDC provides 5 read-only raw-value registers, in which the measurement values VAL0, VAL1 and PRE and the calibration values CAL1 and CAL2 are stored for readout. The width of all raw-value registers is 16 bit. The registers can be read out via the processor interface. For addressing the raw-value registers refer to Chapter 7.1. Please note, that the raw-values are valid only and can be read out only as long as the VALID-flag is set to '1'.

6.5 Processor Interface

The access to the Control- and Status-Register as well as the access to the raw-value registers is controlled by the processor interface, either via the **Parallel Interface** or the **Serial Peripheral Interface (SPI)** depending on pin EN_ SPI (0 = Parallel Interface, 1 = SPI).

In addition to data- and control lines the processor interface provides **flags** to indicate the end of a measurement and to indicate an overflow of the TDC-Core or the Precounter.

6.5.1 Parallel Interface

6.5.1.1 Data- and Control Lines

The Parallel Interface of the TDC-Mach330 provides the following data- and control lines:

- DATA[7:0]: Bi-directional data bus
- CSN: Chip select (low active)
- RDN: Read strobe (low active)
- WRN: Write strobe (low active)
- ADR[2:0]: Address bus

In principle, all controllers addressing a SRAM directly are connectable to the TDC's processor interface, e.g. RENESAS H8-Controller.

6.5.1.2 Timing Diagrams

Figure 6.4 and Figure 6.5 show the read and write cycle timings. The associated read and write cycle timing characteristics are specified in Table 6.1.

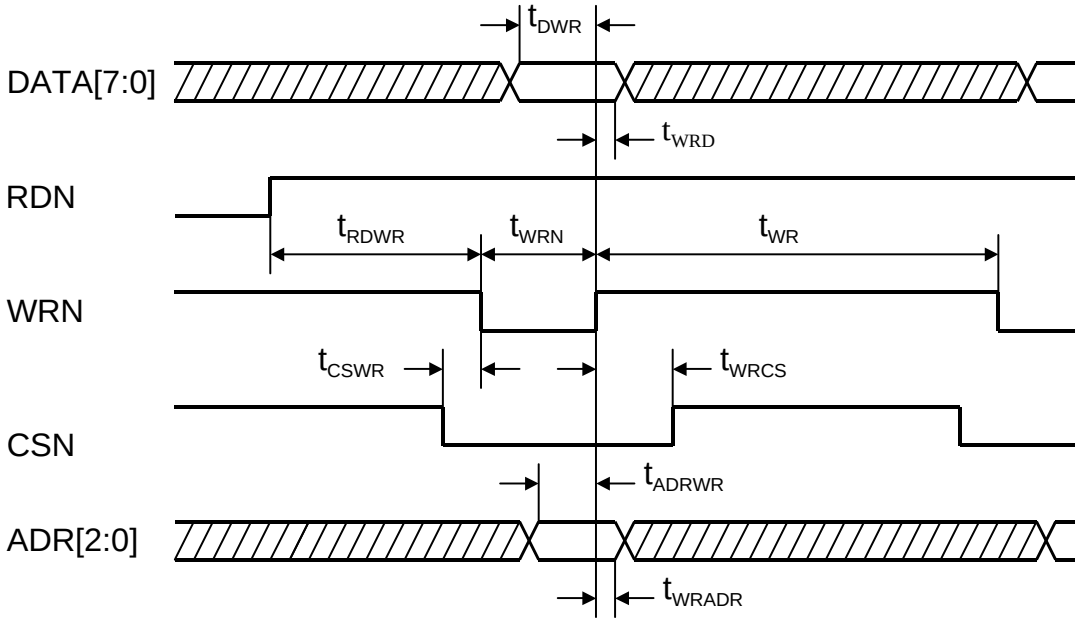


Figure 6.4: Write Cycle Timing

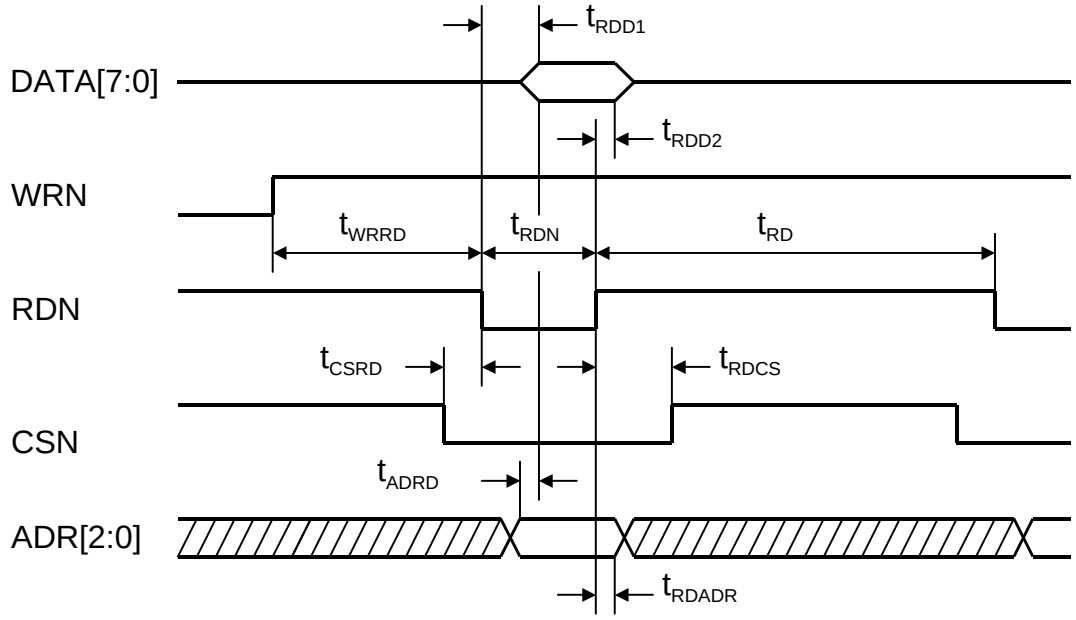


Figure 6.5: Read Cycle Timing

Parameter	Min	Max	Unit
t_{WRN}	25	-	ns
t_{WR}	25	-	ns
t_{DWR}	10	-	ns
t_{WRD}	3	-	ns
t_{ADRWR}	10	-	ns
t_{WRADR}	3	-	ns
t_{CSWR}	0	-	ns
t_{WRCS}	0	-	ns
t_{RDWR}	25	-	ns

Parameter	Min	Max	Unit
t_{RDN}	25	-	ns
t_{RD}	25	-	ns
t_{RDD1}	2	18	ns
t_{RDD2}	2	18	ns
t_{ADRD}	-	18	ns
t_{RDADR}	3	-	ns
t_{CSRD}	0	-	ns
t_{RDCS}	0	-	ns
t_{WRRD}	25	-	ns

V_{CC} = 3.0V-3.6V, T_A = 0 to +70°C, Load: 30pF

Table 6.1: Read and Write Cycle Timing Characteristics

6.5.2 Serial Peripheral Interface (SPI)

6.5.2.1 Data- and Control Lines

The SPI of the TDC-Mach330 acts as slave, providing the following data- and control lines:

- MOSI: Serial data line “master out slave in“
- MISO: Serial data line “master in slave out“
- SCK: Serial SPI-clock, provided by the master
- SSN: Slave select (SSN = 0) resp. SPI-reset (SSN = 1)

Master and TDC exchange their data bit by bit via 8-bit data packets on the serial data lines MOSI and MISO, sending the MSB at first and the LSB at last. Each bit of an 8-bit SPI-cycle is transmitted using the rising edge of the SPI-clock SCK and received using the falling edge of SCK. The idle state of SCK is ‘0’. When SSN is ‘1’, then the SPI is in reset and the line MISO is in tristate. When SSN is ‘0’, then the SPI is active and any number of SPI-cycles can be made, running with or without a rest period of SCK.

6.5.2.2 Timing Diagram

Parameter	Min	Max	Unit
t_{SCK}	40	-	ns
t_{SCKH}	20	-	ns
t_{SCKL}	20	-	ns
t_L	20	-	ns
t_T	20	-	ns

Parameter	Min	Max	Unit
t_{SU}	10	-	ns
t_{HD}	10	-	ns
t_D	2	8,5	ns
t_{LT}	2	8	ns
t_{TT}	2	8	ns

V_{CC} = 3.0V-3.6V, T_A = 0 to +70°C, Load: 30pF

Table 6.2: SPI-Cycle Timing Characteristics

Figure 6.6 shows the SPI-cycle timing. The associated timing characteristics are specified in Table 6.2.

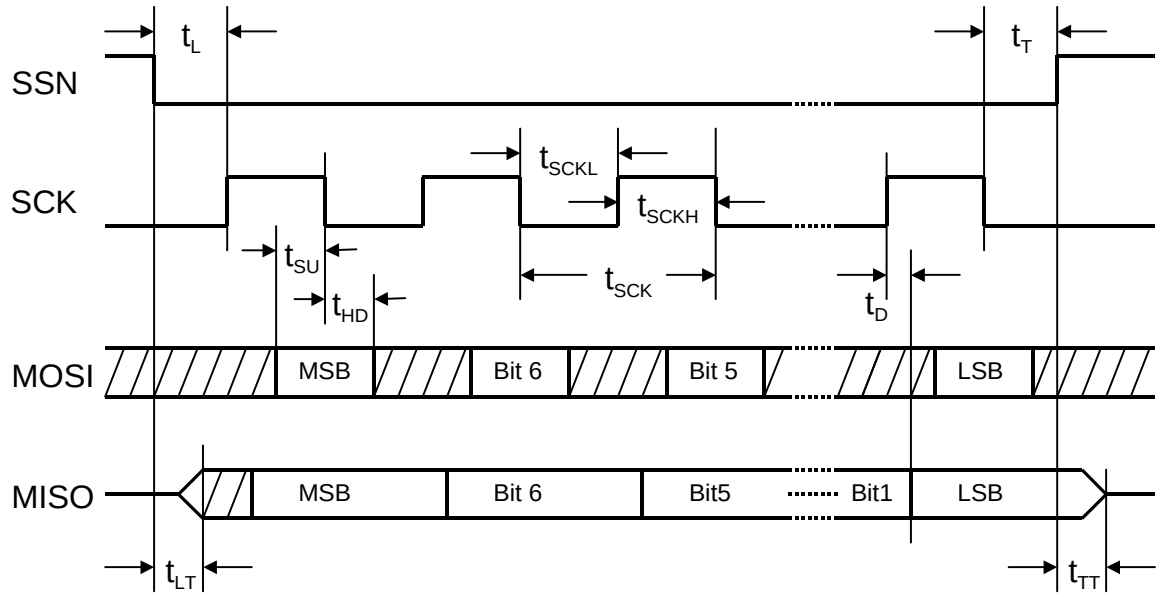


Figure 6.6: SPI-Cycle Timing

6.5.3 Flags

Four flags (VALID, OV_CORE, OV_PRE and OV) are provided, described in Table 6.3. All flags are cleared to ‘0’ on power-on reset or by clearing the Control-Register’s action-bits to ‘0’.

Flag	Description	Location
VALID	0 : No valid data for readout 1 : End of measurement: Raw-value registers contain valid data for readout	Status-Register and Pin VALID
OV_CORE	0 : TDC-Core is ok 1 : Overflow of TDC-Core	Status-Register
OV_PRE	0 : Precounter is ok 1 : Overflow of Precounter	Status-Register
OV	0 : TDC-Core and Precounter are ok 1 : Overflow of TDC-Core or Precounter	Pin OV

Table 6.3: Flags

7 Programming of the TDC-Mach330

7.1 Addressing

7.1.1 Parallel Interface

Accessing the TDC's Control- and Status-Register and reading out the TDC's raw-values is done via the Parallel Interface when pin EN_SPI is '0'. The relevant data is read and written via the bi-directional data bus DATA[7:0]. Addressing of all the registers, shown in Table 7.1, is done via the address bus ADR[2:0]. Each 16 bit raw-value has to be read out by two consecutive read cycles on the same address. The first cycle reads out the low byte, the second cycle reads out the high byte.

Address ADR[2:0]		Register	writable (w) readable (r)
hex	bin		
0x00	000	CAL1 -> low byte first	r
0x01	001	CAL2 -> low byte first	r
0x02	010	VAL0 -> low byte first	r
0x03	011	VAL1 -> low byte first	r
0x04	100	PRE -> low byte first	r
0x05	101	-	-
0x06	110	STATUS_REG	r
0x07	111	CTRL_REG	w / r

Table 7.1: Register Addresses

7.1.2 Serial Peripheral Interface (SPI)

Accessing the TDC's Control- and Status-Register and reading out the TDC's raw-values is done via the SPI when pin EN_SPI is '1'. Master and TDC exchange their data via 8-bit data packets on the serial data lines MOSI and MISO, sending the MSB at first and the LSB at last. As shown is Table 7.2 the information for writing into or reading out the TDC is coded within the two upper-most bits of a MOSI data packet.

Writing into the Control-Register needs only one SPI-cycle: The lowest 6 bits of a MOSI data packet are clocked into the Control-Register using the eighth (= last) falling SCK-edge of the cycle.

Reading out the TDC's Control- and Status-Register needs two SPI-cycles: Within the first cycle the lowest 6 bits of a MOSI data packet are used as register address. Within the second cycle the data of the addressed register is transferred via line MISO. Please make sure, that SSN is set to '0' all the time between the two SPI-cycles.

Reading out the TDC's raw-value registers needs three SPI-cycles: Within the first cycle the lowest 6 bits of a MOSI data packet are taken as register address. Within the second cycle the low byte of the addressed register is transferred via line MISO. In order to read out the register's high byte

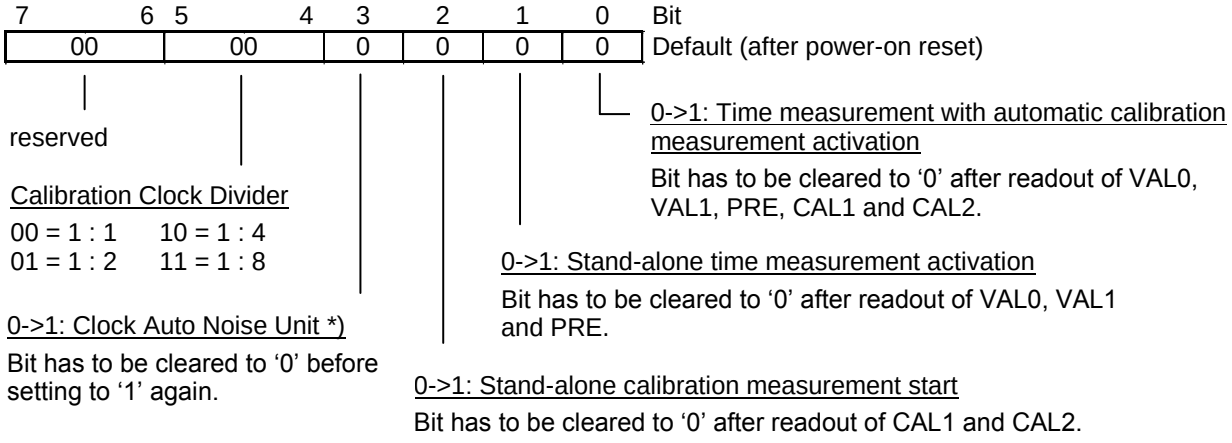
within the third cycle, the register's address has to be transmitted once more within the second cycle. Please make sure, that SSN is set to '0' all the time between the three SPI-cycles.

MOSI data packet (bin) MSB LSB	Register	write (w) read (r)
0000 0000	CAL1 -> low byte first	r
0000 0001	CAL2 -> low byte first	r
0000 0010	VAL0 -> low byte first	r
0000 0011	VAL1 -> low byte first	r
0000 0100	PRE -> low byte first	r
0000 0101	-	-
0000 0110	STATUS_REG	r
0000 0111	CTRL_REG	r
01xx xxxx	CTRL_REG	w

Table 7.2: MOSI data packet format

7.2 Register Format

7.2.1 Control-Register CTRL_REG


7 6 5 4 3 2 1 0 Bit
00 00 0 0 0 0 Default (after power-on reset)
reserved
Calibration Clock Divider
00 = 1 : 1 10 = 1 : 4
01 = 1 : 2 11 = 1 : 8
0->1: Clock Auto Noise Unit *)
Bit has to be cleared to '0' before setting to '1' again.
0->1: Time measurement with automatic calibration measurement activation
Bit has to be cleared to '0' after readout of VAL0, VAL1, PRE, CAL1 and CAL2.
0->1: Stand-alone time measurement activation
Bit has to be cleared to '0' after readout of VAL0, VAL1 and PRE.
0->1: Stand-alone calibration measurement start
Bit has to be cleared to '0' after readout of CAL1 and CAL2.

*) - *Warning: Reading out bit 3 will always show a '0', no matter if bit 3 is set to '1' or cleared to '0'.*

- *Setting bit 3 to '1' can be done along with clearing bit 0, 1 or 2 to '0'. Clearing bit 3 to '0' can be done along with setting bit 0, 1 or 2 to '1'.*

Figure 7.1: Control-Register CTRL_REG Format

tdc@msc-ge.com www.msc-ge.com

7.2.2 Status-Register STATUS_REG

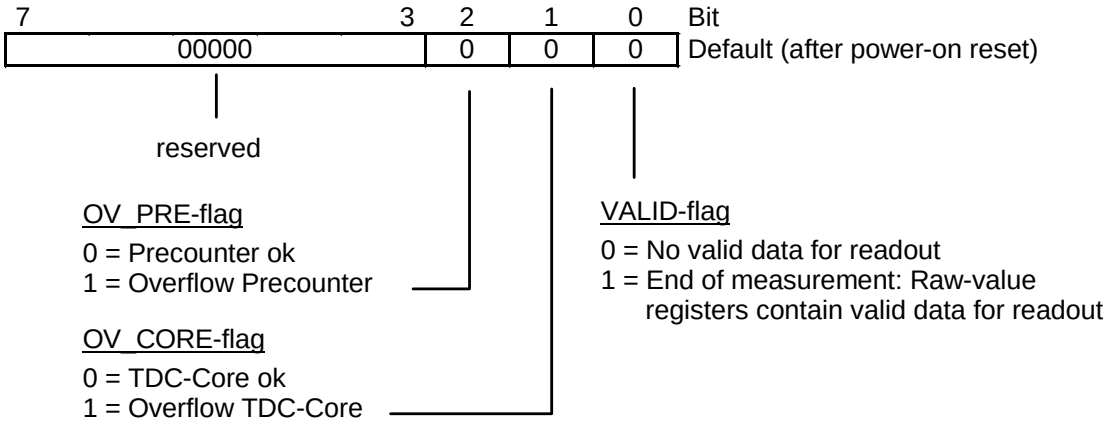


Figure 7.2: Status-Register STATUS_REG Format

7.2.3 Raw-Value Registers

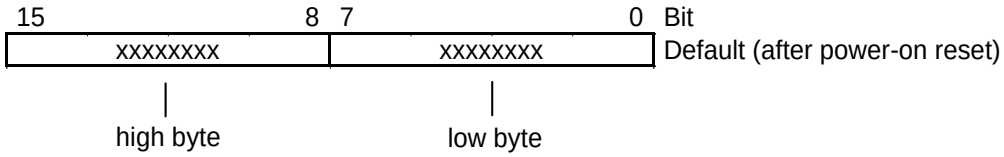


Figure 7.3: Raw-Value Register Format

All raw-values are 16 bit UNSIGNED INTEGER numbers. Thus, the maximum number for the measurement- and calibration values VAL0, VAL1, CAL1 and CAL2 is 0xffff = 65535. Because the MSB of PRE is fixed to '0' at all times, it's maximum number is 0x7fff = 32767. To read out a complete raw-value via the 8-bit processor interface two read cycles are necessary (see Chapter 7.1). The raw-value registers are not resettable, so there default state is undefined after power-on reset.

8 Sleep Mode

The TDC-Mach300 provides a Sleep Mode that allows standby current to be reduced dramatically during periods of system inactivity. Sleep Mode is controlled by the SLEEPN pin.

During Sleep Mode the TDC is not operational, the contents of the registers is not maintained and the I/Os are tristated. In Sleep mode power supply is in its normal operating range, eliminating the need for external switching of the power supply. Table 8.1 compares the characteristics of Normal Mode, Off Mode and Sleep Mode.

Characteristic	Normal Mode	Off Mode	Sleep Mode
SLEEPN pin	high	-	low
Static Current I_{CC}/I_{CS} *)	24mA (typical)	0	21µA (typical)
Supply Voltage V_{CC}	normal range	0	normal range
Logic operation	TDC	not operational	not operational
I/O operation	see Pin/Ball Function Lists, Chapter 4.3	tristated	tristated
Register contents	maintained	not maintained	not maintained

*) see Table 9.2

Table 8.1: Characteristics of Normal, Off and Sleep Modes

Typically, the TDC enters Sleep Mode several hundred nanoseconds after SLEEPN is held at a valid low and restarts normal operation as specified in Figure 8.1. The associated timing characteristics are specified in Table 8.2. After leaving Sleep Mode and reaching Normal Mode first of all a low-active reset pulse has to be performed at the RSTN pin. The pulse has to be 100ns at least. After this reset the TDC has its default settings.

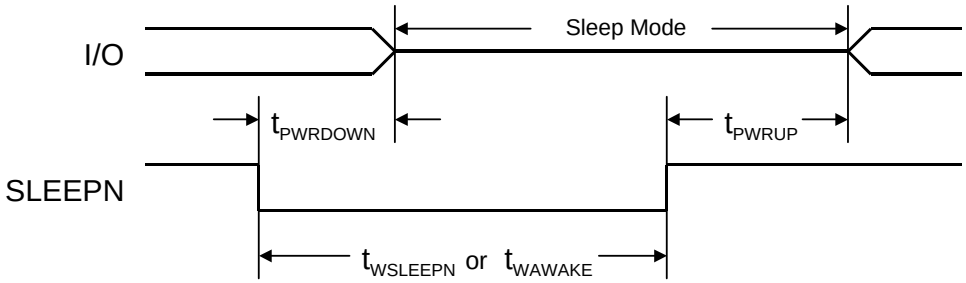


Figure 8.1: Sleep Mode Timing

Symbol	Parameter	Min	Max	Unit
$t_{PWRDOWN}$	SLEEPN low to power down	-	400	ns
t_{PWRUP}	SLEEPN high to power up	-	600	µs
$t_{WSLEEPN}$	SLEEPN pulse width	400	-	ns
t_{WAWAKE}	SLEEPN pulse rejection	-	100	ns

Notes: - Do not enter Sleep Mode during power-on device configuration (cp. Chapter 9.8).
- SLEEPN has a glitch filter to prevent false triggering

Table 8.2: Sleep Mode Timing Characteristics

9 Appendix

9.1 Electrical Specification

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3.135	3.3	3.465	V
T_{JCOM}	Junction Temperature Commercial Operation	0	-	85	°C

Table 9.1: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{CI}	PLD-Configuration Current	V_{CC} = 3.3V, T_A = 25°C	-	38	-	mA
I_{CC}	Standby Current	V_{CC} = 3.3V, T_A = 25°C	-	24	-	mA
I_{CS}	Sleep Mode Current	V_{CC} = 3.3V, T_A = 25°C	-	21	-	µA
I_{CM}	Current during Measurement	T_A = 25°C	-	1.5	-	mA
I_{CP}	Current of CALCLK-Pin when Crystal Clock is active	V_{CC} = 3.3V, T_A = 25°C, f_{CALCLK} = 4MHz	-	0.6	-	mA
I_{IL}	Input or I/O Leakage Low	0 ≤ V_{IN} ≤ (V_{CC} - 0.2V)	-	-	10	µA
I_{IH}	Input or I/O Leakage High	(V_{CC} - 0.2V) < V_{IN} ≤ 3.6V	-	-	40	µA
V_{IL}	Input Low Voltage		-0.3	-	0.8	V
V_{IH}	Input High Voltage		2.0	-	3.6	V
V_{OL}	Output Low Voltage		-	-	0.4	V
V_{OH}	Output High Voltage		V_{CC}-0.4	-	-	V
I_{OL}	Output Low Current		-	8	-	mA
I_{OH}	Output High Current		-	-8	-	mA
I_{PU}	I/O Active Pull-up Current	0 ≤ V_{IN} ≤ 0.7 V_{CC}	-30	-	-150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (Max) ≤ V_{IN} ≤ V_{IH} (Max)	30	-	150	µA
C1	I/O Capacitance	V_{CC} = 3.3V, V_{IO} = 0 to V_{IH} (Max), T_A = 25°C, f = 1.0MHz	-	8	-	pF
C2	Dedicated Input Capacitance	V_{CC} = 3.3V, V_{IO} = 0 to V_{IH} (Max), T_A = 25°C, f = 1.0MHz	-	8	-	pF

NOTES: - *Over recommended Operation Conditions* - *All I/Os are LVCMOS (3.3V)*
- $I_{CP} \approx 160\mu A / MHz * f_{CALCLK} * (V_{CC} / 3.3V)^2$

Table 9.2: Electrical Characteristics

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.5	3.75	V
V_{IN}	Dedicated Input Voltage Applied	-0.5	4.25	V
V_{IOT}	I/O Tristate Voltage Applied	-0.5	3.75	V
T_{STRG}	Storage Temperature	-65	150	°C
T_J	Junction Temperature	-	125	°C

***NOTE**: Stresses above these values may cause permanent damage to the device.*

Table 9.3: Absolute Maximum Ratings

9.2 Resolution (LSB)

9.2.1 How to calculate the Resolution

The TDC's resolution $\mathbf{RES_{LSB}}$ is calculated using the divided calibration clock period $\mathbf{t_{CAL}}$ and the calibration values **CAL1** and **CAL2**:

$$\mathbf{(A1)} \qquad \mathbf{RES_{LSB} = t_{CAL} / (CAL2 - CAL1)}$$

9.2.2 Voltage and Temperature Dependance

Table 9.4 shows the supply voltage and ambient temperature dependance of the TDC's resolution, arised from averaging the measured resolution of numerous TDCs.

Supply Voltage V_{CC} [V]	Resolution RES_{LSB} [ps] at T_A =			
	0°C	25°C	50°C	70°C
3,0	111	113	114	116
3,3	113	115	118	120
3,6	113	117	119	121

Table 9.4: Resolution Voltage and Temperature Dependance

9.3 Differential Non-Linearity

The quality of a measurement not only depends on the TDC's resolution but also on its so-called **differential non-linearity (DNL)**. The DNL is a criterion for the variation of the quantisation stage's width (LSB-width).

Figure 9.1 shows a typical histogram of the TDC's LSB-widths at V_{CC} = 3.3V, where the average LSB-width is identical with the resolution RES_{LSB}. Furthermore the figure illustrates the definition of the DNL.

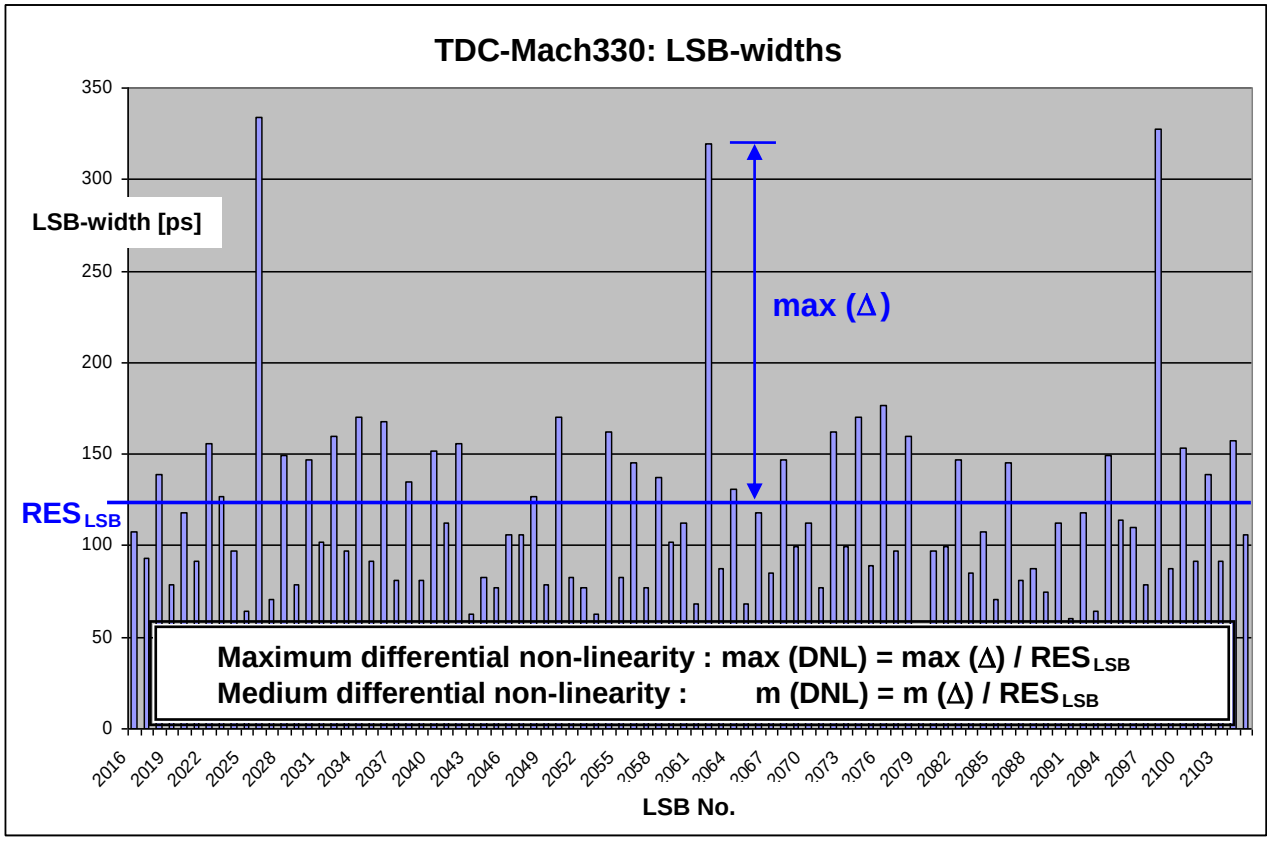

TDC-Mach330: LSB-widths
LSB-width [ps]
max (Δ)
RES LSB
Maximum differential non-linearity : max (DNL) = max (Δ) / RES LSB
Medium differential non-linearity : m (DNL) = m (Δ) / RES LSB
LSB No.

Figure 9.1: Resolution, LSB-Width and Differential Non-Linearity

Table 9.5 shows the maximum and medium differential non-linearity, based upon measurements of several TDCs at different supply voltages.

m (DNL)	max (DNL)
30 %	150 %

Table 9.5: Differential Non-Linearity ($T_A \approx 25°C$)

9.4 Minimum and Maximum Measurement Period

The minimum and maximum measurement periods depend on the divided calibration clock period $\mathbf{t_{CAL}}$ (cp. Chapter 5.2 and Chapter 6.1).

9.4.1 Minimum Measurement Period

As shown in Chapter 5.1 each time measurement is divided into three stages. At the end of the first measurement stage the TDC-Core has to be reactivated automatically for the third measurement stage. Only after this time the TDC will detect a stop-signal. Therefore the minimum measurement period $\mathbf{t_{MIN}}$ of the TDC is:

$$\textbf{(A2)} \qquad t_{MIN} = 1{,}5 * t_{CAL} + 100ns$$

Stop-signals which don't meet the minimum measurement period, are detected sometimes, but not always.

As mentioned in Chapter 6.1, the maximum frequency of the divided calibration clock is limited to 4MHz. Therefore an ultimate minimum measurement period of 475ns can be achieved.

9.4.2 Maximum Measurement Period

The maximum measurement period $\mathbf{t_{MAX}}$ is defined by the 15 bit wide Precounter:

$$\textbf{(A3)} \qquad t_{MAX} = 2^{15} * t_{CAL}$$

As mentioned in Chapter 6.1, the minimum frequency of the divided calibration clock is limited to 3MHz. Therefore an ultimate maximum measurement period of about 10,9ms can be achieved.

9.5 Minimum Pulse Width of Start- and Stop-Signals

The minimum pulse width $\mathbf{t_s}$ of signals on the start- and stop-inputs START and STOP is:

$$\textbf{(A4)} \qquad t_S = 6ns$$

The time t_s is relevant for both, high- and low-level of the signals.

9.6 Timing when Activating a Time Measurement

Figure 9.2 shows the timing of the TDC's pins SCK, WRN and START when activating a time measurement via the parallel interface resp. via the SPI by setting bit 0 or bit 1 to '1' within the Control-Register. In Table 9.6 the associated characteristics are specified.

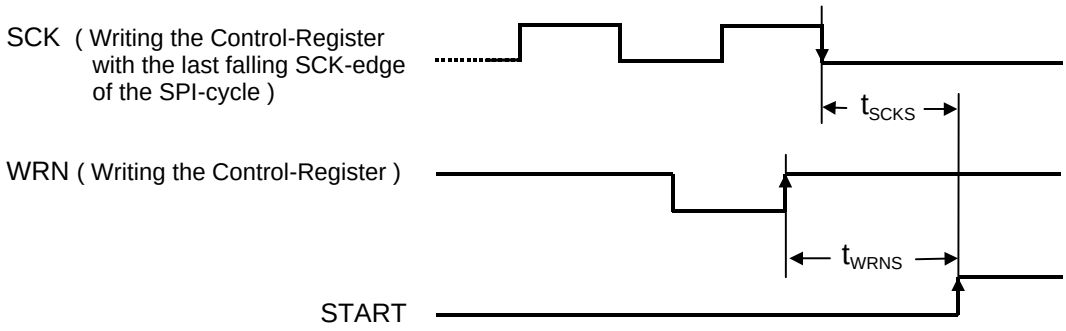

SCK (Writing the Control-Register with the last falling SCK-edge of the SPI-cycle)
tSCKS
WRN (Writing the Control-Register)
tWRNS
START

Figure 9.2: Timing when activating a Time Measurement

Symbol	Parameter	Min	Typ	Max	Unit
t_{WRNS}	Parallel IF: Setup time for start detection	3,5	-	13	ns
t_{SCKS}	SPI: Setup time for start detection	5,5	-	20	ns

Table 9.6: Timing Characteristics when activating a Time Measurement

9.7 Dead Times

Due to the measurement principle the TDC-Mach330 has got a dead time after the execution of a time measurement. During this time period the start and stop detection of the TDC-Core and the Precounter is disabled because of post-processing and storing the measurement- and precounter values into the raw-value registers. So reading out the TDC and initiating a new measurement cycle for another time- and/or calibration measurement before the end of dead time is unwise.

Due to the fact that the TDC's core and precounter are not available for time measurements during automatic or stand-alone calibration measurements, this time periods are also treated as dead times.

9.7.1 Dead Time of a stand-alone Time Measurement

The dead time $\mathbf{t_{TOT\_M}}$ of a time measurement without automatic calibration measurement is defined as the time period between the stop-signal at the TDC-pin STOP and the rising edge of the VALID-flag at pin *) VALID.

The dead time $\mathbf{t_{TOT\_M}}$ depends on the divided calibration clock period $\mathbf{t_{CAL}}$ (cp. Chapter 5.2). Its maximum value is calculated as follows:

$$\textbf{(A5)} \qquad \mathbf{t_{TOT\_M} = 1{,}5 * t_{CAL} + 115ns}$$

9.7.2 Dead Time of a stand-alone Calibration Measurement

When using the parallel interface the dead time $\mathbf{t_{TOT\_C}}$ of a stand-alone calibration measurement is defined as the time period between the rising edge of the write strobe at TDC-pin WRN when activating the corresponding action-bit within the Control-Register and the rising edge of the VALID-flag at pin *) VALID.

When using the SPI the dead time $\mathbf{t_{TOT\_C}}$ is defined as the time period between the last falling SCK-edge of the SPI-cycle when writing the Control-Register and the rising edge of the VALID-flag at pin *) VALID.

The dead time $\mathbf{t_{TOT\_C}}$ depends on the period $\mathbf{t_{CAL}}$ of the divided calibration clock (cp. Chapter 5.2). Its maximum value is calculated as follows:

$$\textbf{(A6)} \qquad \mathbf{t_{TOT\_C} = 5{,}5 * t_{CAL} + 130ns}$$

9.7.3 Dead Time of a Time Measurement with autom. Calibration Measurement

The dead time $\mathbf{t_{TOT\_MC}}$ of a time measurement with automatic calibration measurement is defined as the time period between the stop-signal at the TDC-pin STOP and the rising edge of the VALID-flag at pin *) VALID.

The dead time $\mathbf{t_{TOT\_MC}}$ depends on the period $\mathbf{t_{CAL}}$ of the divided calibration clock (cp. Chapter 5.2). Its maximum value is calculated as follows:

$$\textbf{(A7)} \qquad \mathbf{t_{TOT\_MC} = 7 * t_{CAL} + 215ns}$$

*) *Load: 30pF*

9.8 Power-On Characteristics

A MachXO-PLD is SRAM-based. After switching-on the power supply V_{CC} the device is configured automatically as TDC by loading a program from its internal flash memory. During this PLD-configuration time all I/Os are tri-stated with an internal pull-up resistor enabled. After configuration all TDC-relevant I/Os are activated and operate as shown in Table 4.3.

The PLD-configuration time is defined as the time period between reaching the minimum power supply (V_{CC} = 3.0V) and the activation of the device I/Os. The maximum PLD-configuration time is 600µs.

After device configuration a low-active power-on reset pulse has to be performed at the TDC-pin RSTN. The pulse has to be 100ns at least.

After power-on reset the TDC has its default settings. Now a measurement cycle can be initiated by setting one of three action-bits to ‘1’ within the TDC’s Control-Register (see Chapter 5.4).

9.9 Board Layout Recommendations

9.9.1 General Power and Ground Recommendations

To guarantee a high degree of signal integrity a power and a ground plane are a must for layout. The power plane must have low resistance to ensure minimum voltage drop to the devices. Furthermore it is strongly recommended to isolate the TDC's power supply plane from the supply plane of all other components. This can be done either by using a separate voltage regulator for the TDC's supply or by placing a Ferrite Bead with good current carrying characteristics and low resistance in series with the voltage source to choke off the high frequency noise that may be caused by the other shared power supply.

9.9.2 Decoupling Recommendations

Decoupling or bypass capacitors play a big role in the TDC's performance. The main role of bypass capacitors is to act as a local DC power supply to meet the demands of fluctuating power - especially when the measurement starts - and block unwanted noise coming from or going into the power plane.

The following guideline is a good rule of thumb for proper decoupling:

- Bypass capacitor usage must take into account both a low ESR and a low ESL.
- Use four 100nF X7R-ceramic-capacitors (0805 or 0603), one each side of the TDC, and one 2.2nF X7R-ceramic-capacitor (0805 or 0603) per power pin.
- Locate decoupling capacitors as close as possible to the device power pins and run short, wide traces to vias when they are required.
- Use two 10µF tantalum electrolytic capacitors to help eliminate low frequency coupling and maintain a low impedance power system.
- Use a large 220µF tantalum electrolytic capacitor at power source.

9.10 Measurement Results

9.10.1 Singleshot Measurements and RMS Resolution

Table 9.7 shows the **singleshot standard deviation σ**, also referred to as **rms resolution**, depending on the power supply voltage V_{CC}.

In a normal distribution the so-called one-sigma area ±σ contains about 68% of the singleshot measurement results. About 95,5% will fall within the two-sigma area ±2σ.

Power Supply V_{CC} [V]	σ [ps]
3,0	265
3,3	250
3,6	235

Table 9.7: RMS Resolution σ ($T_A \approx 25°C$)

All singleshot standard deviations of Table 9.7 are averaged values, derived from singleshot measurements of several TDCs at the following conditions:

- Measurement period: 9 - 10µs.
- Increment: 1ns.
- Sampling rate: One measurement per measuring point.
- Calibration clock: f_{CAL} = 4 MHz.
- Automatic calibration measurement after time measurement.
- Supply voltage: 3.0V, 3.3V and 3.6V.
- Temperature: approx. 25°C.
- Reference: Universal Time Interval Counter SR620 (Stanford Research Systems).

Figure 9.3 shows exemplarily the TDC's measurement errors of singleshot measurements for a measurement period from 9 to 10µs at 3,3V. The Universal Time Interval Counter SR620 (RMS resolution ≈ 25ps) is used for reference measurements. The offset of the diagram is approx. 700ps. This systematic error results from a different length of cables for start and stop and is irrelevant here.

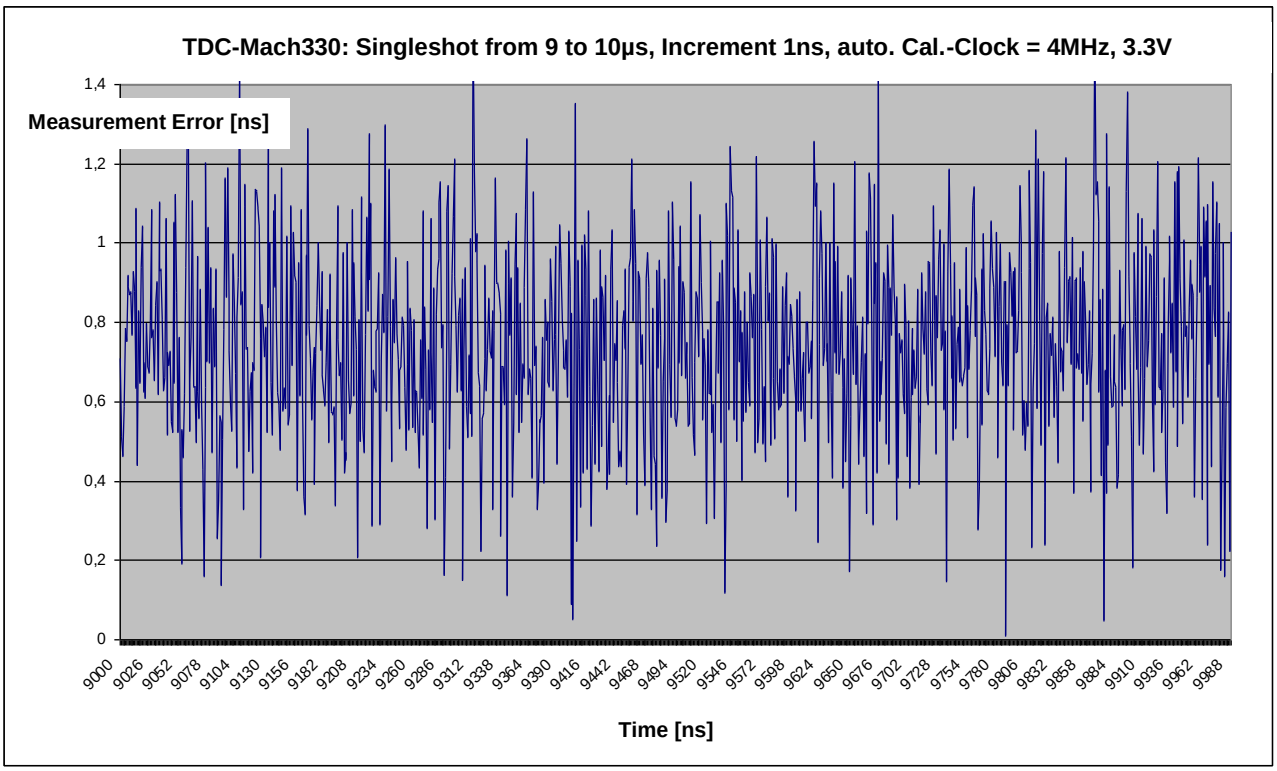


Figure 9.3: Measurement Errors of Singleshot Measurements at 3,3V

9.10.2 Auto Noise Unit: Effect on Measurement Errors

If there is the possibility to measure the same time difference several times a higher accuracy can be achieved by calculating the average measurement result. With an increasing number of measurements the average measurement result will converge the real time difference. So, in theory, the measurement error of the average measurement result is getting smaller and smaller. In practice, however, a satisfying accuracy will not be achieved if systematic errors are not eliminated or minimized by averaging.

Figure 9.4 and Figure 9.5 show the TDC's measurement errors of the average measurement results from 16 measurements per time difference for a measurement period from 9 to 10µs with an increment of 1ns. The measurements of Figure 9.4 are made without using the Auto Noise Unit; the measurements of Figure 9.5 are made using the Auto Noise Unit.

In Figure 9.4 the standard deviation of the average measurement results is improved by almost $1/\sqrt{16}$ from σ=240ps (singleshot standard deviation of Figure 9.3) down to σ_{16}=61ps. However, using the Auto Noise Unit (Figure 9.5) results in an even better standard deviation of σ_{16}=56ps.

The reason for this difference is the quantisation of the TDC-Core's characteristic (cp. Chapter 6.2.3): If assuming that the start-signal and the calibration clock are totally asynchronous to each other and that the stop-signal and the calibration clock are asynchronous to each other as well, then measuring exactly the same time difference many times will lead to different measurement values VAL0 and VAL1 each time. If the Auto Noise Unit is not used, then all associated calibration measurements will sample always the same quantisation stages. So, in contrast to VAL0 and VAL1, the calibration values CAL1 and CAL2 are always the same and averaging will not eliminate their

quantisation errors. Using the Auto Noise Unit results in an improved standard deviation because not only the quantization errors of the measurement values but also those of the calibration values are eliminated.

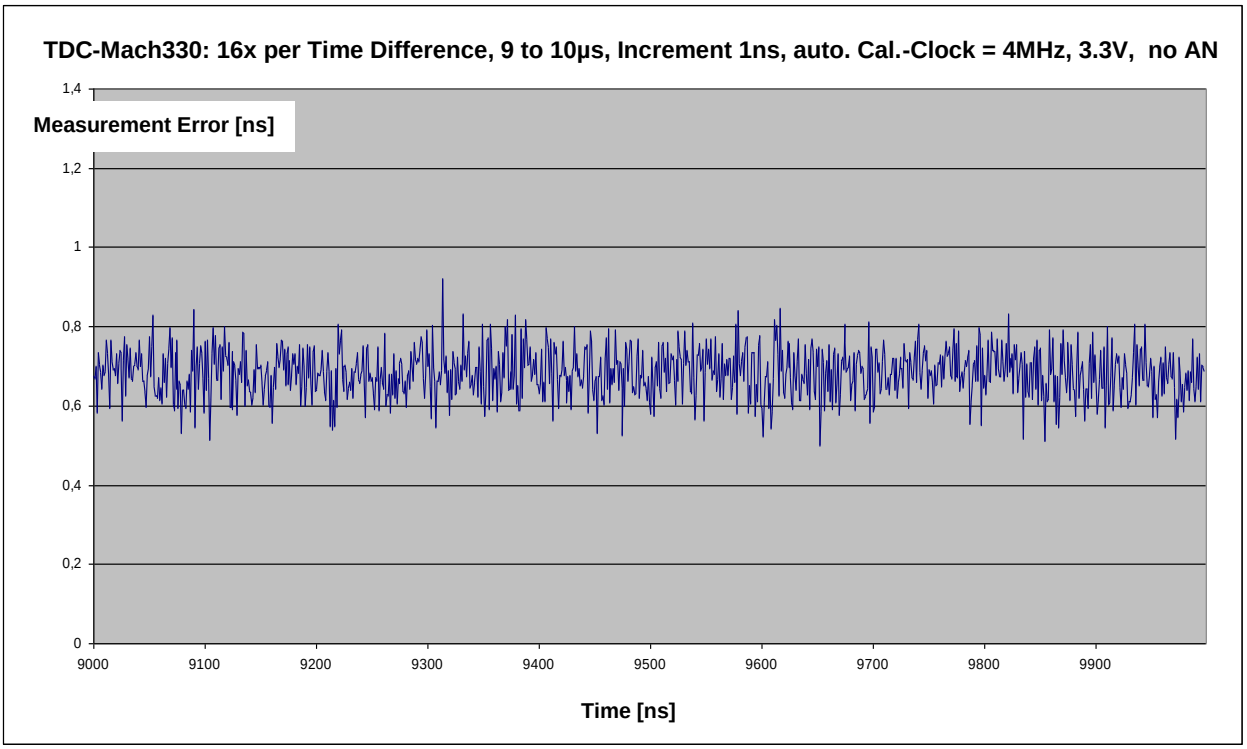


Figure 9.4: Measurement Errors of average Measurement Results (16x, without Auto Noise)

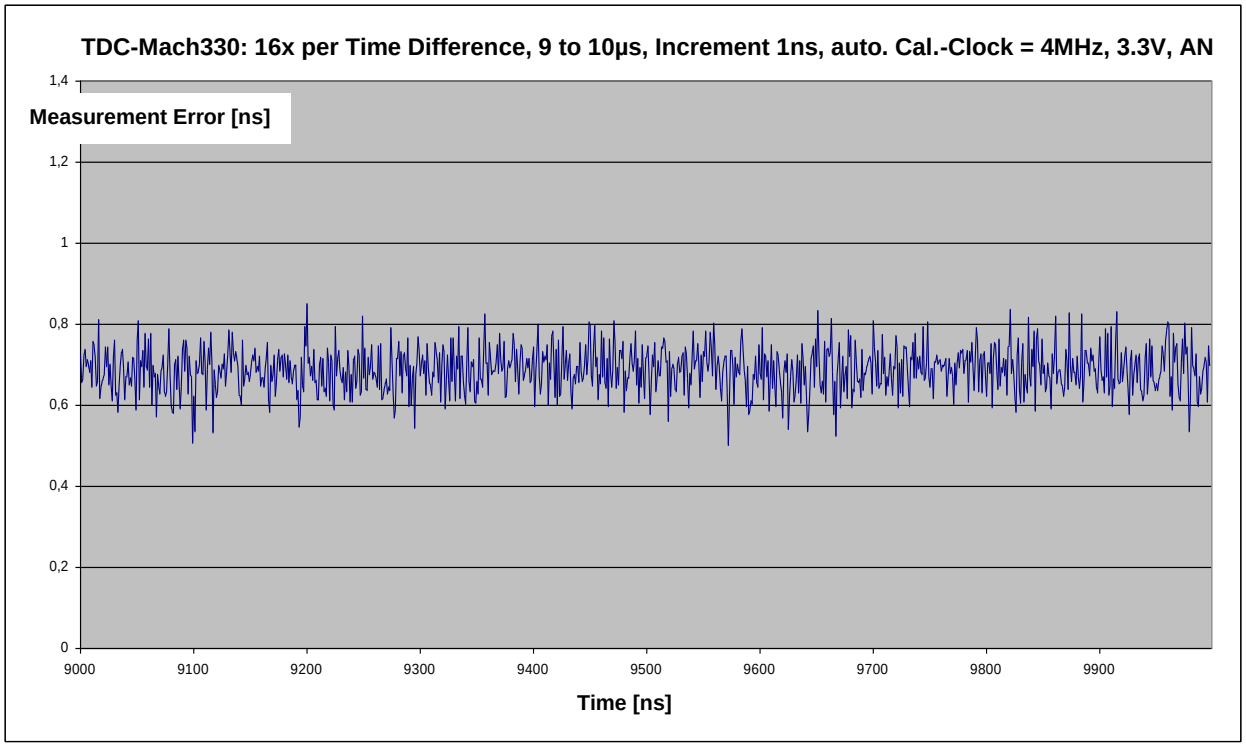


Figure 9.5: Measurement Errors of average Measurement Results (16x, with Auto Noise)

Figure 9.6 and Figure 9.7 show the TDC's measurement errors with 64 and 128 measurements per time difference, using the Auto Noise Unit. The standard deviation of the average measurement results is $\sigma_{64} = 31ps$ resp. $\sigma_{128} = 22ps$.

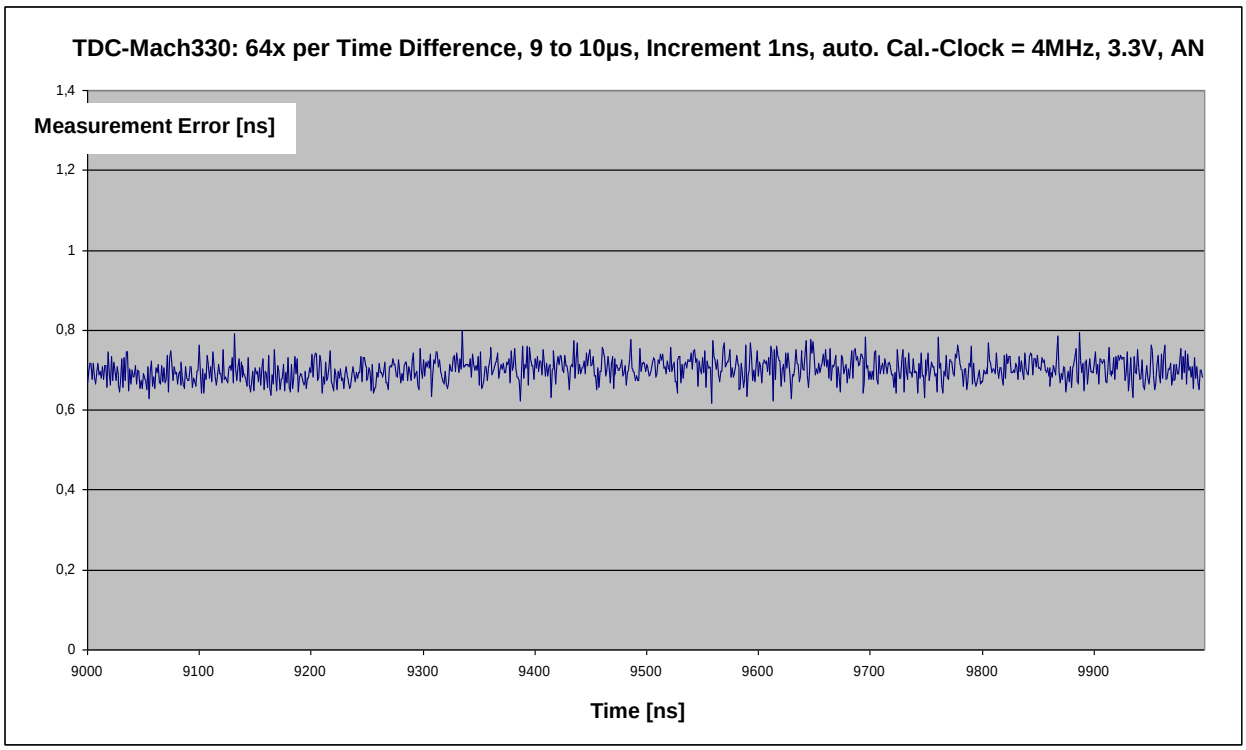


Figure 9.6: Measurement Errors of average Measurement Results (64x, with Auto Noise)

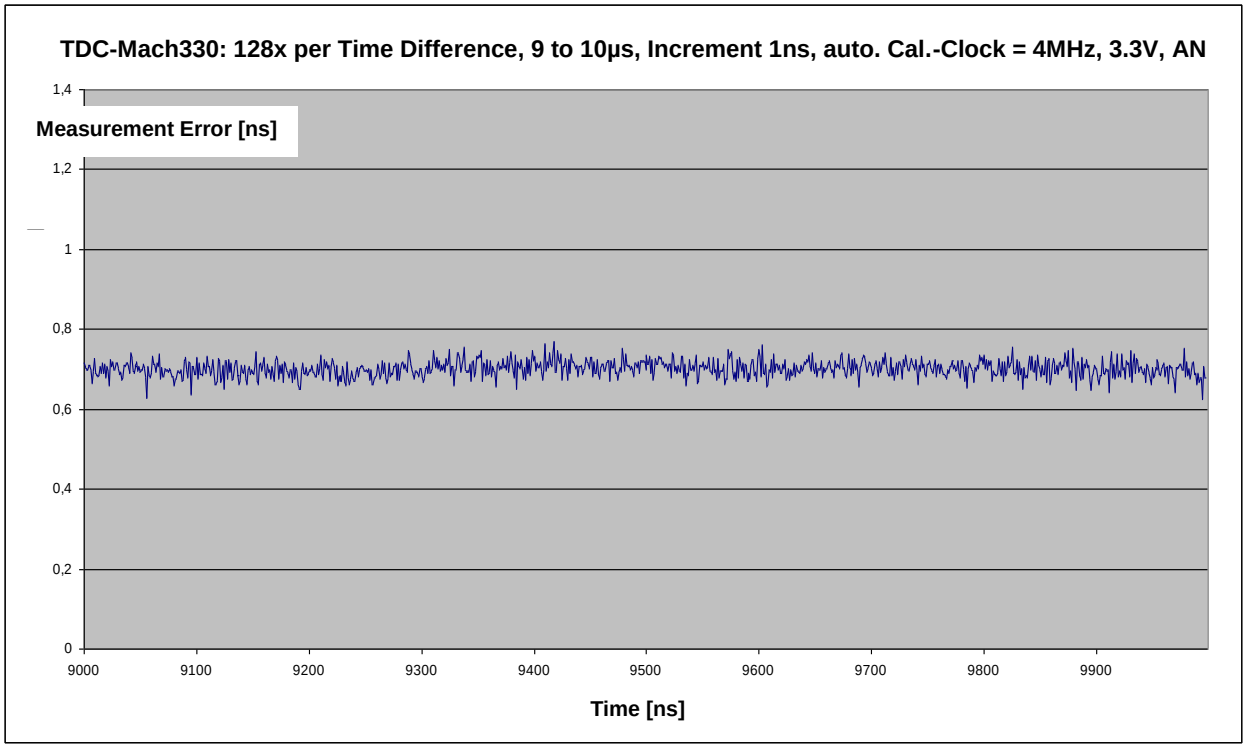


Figure 9.7: Measurement Errors of average Measurement Results (128x, with Auto Noise)